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FILED UNDER 35 U.S.C. 371

PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10069419	04/12/2002	~~438~~ 235	492.000	~~2871~~ 2812	Harold Pitts

**APPLICANTS: Fannasch Lothar;

**CONTINUING DATA VERIFIED:

THIS APPLICATION IS A 371 OF PCT/DE00/02889 08/24/2000

** FOREIGN APPLICATIONS VERIFIED:

GERMANY 199 40 480.1 08/26/1999

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐	
Foreign priority claimed	☐ yes ☐ no		ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no		048662-0129
Verified and Acknowledged Examiners's intials			

TITLE : Conductor track supporting layer for laminating inside a chip card, chip card comprising a conductor track supporting layer, and method for producing a chip card

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING		
Amount Due	Date Paid		Sheets Drwg.	Figs.Drwg.	Print Fig.
		Primary Examiner			
☐ TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner		

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